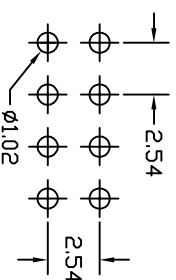
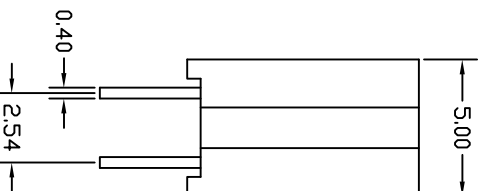
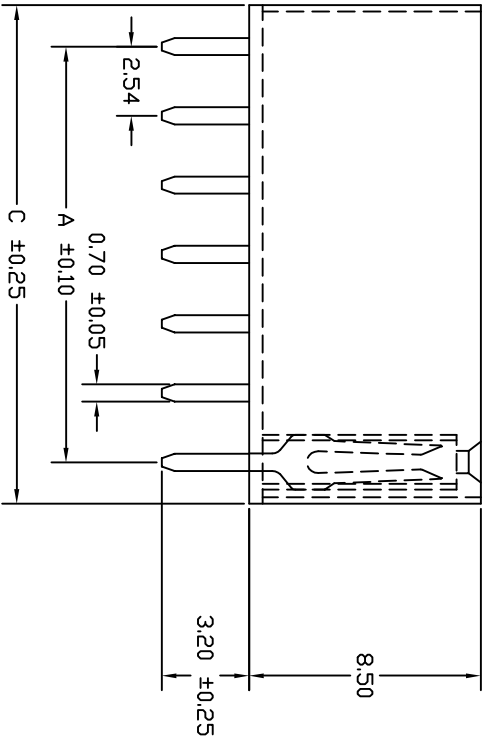
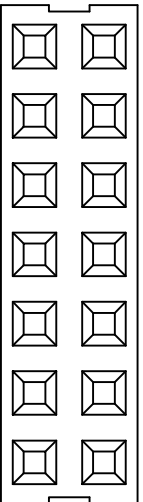


No. of Positions	A	C
2	2.54	5.58
3	5.08	8.12
4	7.62	10.66
5	10.16	13.20
6	12.70	15.74
7	15.24	18.28
8	17.78	20.82
9	20.32	23.36
10	22.86	25.90
11	25.40	28.44
12	27.94	30.98
13	30.48	33.52
14	33.02	36.06
15	35.56	38.60
16	38.10	41.14
17	40.64	43.68
18	43.18	46.22
19	45.72	48.76
20	48.26	51.30
21	50.80	53.84
22	53.34	56.38
23	55.88	58.92
24	58.42	61.46
25	60.96	64.00
26	63.50	66.54
27	66.04	69.08
28	68.58	71.62
29	71.12	74.16
30	73.66	76.70
31	76.20	79.24
32	78.74	81.78
33	81.28	84.32
34	83.82	86.86
35	86.36	89.40
36	88.90	91.94
37	91.44	94.48
38	93.98	97.02
39	96.52	99.56
40	99.06	102.10



Recommended P.C. Board
Hole Layout

Note:
Selective plating: gold plated on contact area,
Tin on solder area

SPECIFICATIONS

Current Rating: 3 Amps
 Insulator resistance: 5000 Megohms min.
 Contact resistance: 20 m ohms max.
 Dielectric withstanding: AC 1000 V
 Operating Temperature: -40°~+125°C
 Contact Material: Phosphor bronze
 Insulator Material: PBT, UL94V-0
 Plating: Tin, Gold or Selectively plated

replace "xx" with number of positions (not total pins) to complete P/N

REV	DATE	BY	DESCRIPTION
A	6-11-03	BC	CORRECTED PIN DIMENSIONS

Sullins Electronics San Marcos, CA www.SullinsElectronics.com		GENERAL TOLERANCE	SCALE	NTS	DRAWN	BC	DATE	DWG. NO.	TITLE	REV.
XX ±	XXX ±	MM	MM	CHECK	DATE	6043A	2.54mm FEMALE HEADER	A		
X ± 0.20	.XXX ±	APPROVE	DATE	PP_Cxx2LFBN	8.50mm Profile	1/1				
X ± 0.10	X' ±	DATE	PP_Cxx2LFBN	8.50mm Profile	1/1					
.XX ± 0.05	X' ±	DATE	PP_Cxx2LFBN	8.50mm Profile	1/1					